

## **AMENDMENTS TO THE CLAIMS**

Please amend the claims as follows:

- 1 1. (currently amended) A content addressable memory (CAM) device comprising:  
2 a first plurality of storage circuits to store an upper value;  
3 a second plurality of storage circuits to store a lower value; and  
4 a plurality of compare circuits to determine if a first comparand value is within a range of  
5 values defined by the upper value and the lower value, wherein the upper value  
6 comprises a plurality of bits ordered from a most significant bit to a least significant  
7 bit, and wherein each of the plurality of compare circuits is adapted to receive a  
8 respective one of the plurality of bits and to compare the one of the plurality of bits to  
9 a respective bit within the first comparand value; and  
10 a match line, wherein a most significant compare circuit of the plurality of compare circuits  
11 is coupled to the match line, the most significant compare circuit including circuitry  
12 to affect a logical state of the match line if either (1) a most significant bit of the first  
13 comparand value is greater than the most significant bit of the upper value, or (2) the  
14 most significant bit of the first comparand is equal to the most significant bit of the  
15 upper value, and a result signal from a less significant compare circuit of the plurality  
16 of compare circuits indicates that the first comparand value minus the value  
17 represented by the most significant bit of the first comparand value is greater than the  
18 upper value minus the value represented by the most significant bit of the upper  
19 value.

- 1 2. (original) The CAM device of claim 1 wherein the first comparand value is a field of bits

2 within a second comparand value.

1 3. (original) The CAM device of claim 1 wherein each of the first plurality of storage circuits  
2 includes a memory element to store at least one bit of the upper value.

1 4. (original) The CAM device of claim 1 wherein each of the plurality of compare circuits  
2 includes circuitry to compare a bit of the first comparand to a bit of the upper value and to  
3 output a result signal in a first state if the bit of the first comparand is greater than the bit of  
4 the upper value and to output the result signal in a second state if the bit of the first  
5 comparand is less than the bit of the upper value.

1 5. (original) The CAM device of claim 4 wherein outputting the result signal in a first state  
2 comprises switchably coupling a match signal line to a predetermined voltage reference to  
3 affect a voltage level of the match signal line.

1 6. (original) The CAM device of claim 5 wherein outputting the result signal in the second  
2 state comprises decoupling the match signal line from the predetermined voltage reference.

1 7. (original) The CAM device of claim 5 wherein coupling the match signal line to a  
2 predetermined voltage reference comprises coupling the match signal line to a ground  
3 voltage reference to pull down the voltage level of the match signal line.

1 8. (original) The CAM device of claim 4 further comprising a match line, and wherein a most  
2 significant compare circuit of the plurality of compare circuits is coupled to the match line,

the most significant compare circuit being adapted to affect a logical state of the match line according to the result signal.

9. (original) The CAM device of claim 8 wherein the most significant compare circuit is coupled to output the result signal to the match line.

10. (original) The CAM device of claim 8 wherein at least one other of the plurality of compare circuits is coupled to output the result signal to the most significant compare circuit.

11. (canceled)

12. (canceled)

13. (currently amended) The CAM device of claim 1 wherein the lower value comprises a plurality of bits ordered from a most significant bit to a least significant bit, and wherein each of the plurality of compare circuits is adapted to ~~store~~receive a respective one of the plurality of bits and to compare the one of the plurality of bits to a respective bit within the first comparand value.

14. (currently amended) ~~The CAM device of claim 13 further comprising~~ A content addressable memory (CAM) comprising:  
a first plurality of storage circuits to store an upper value;  
a second plurality of storage circuits to store a lower value; and

5 a plurality of compare circuits to determine if a first comparand value is within a range of  
6 values defined by the upper value and the lower value, wherein the lower value  
7 comprises a plurality of bits ordered from a most significant bit to a least significant  
8 bit, and wherein each of the plurality of compare circuits is adapted to receive a  
9 respective one of the plurality of bits and to compare the one of the plurality of bits to  
10 a respective bit within the first comparand value; and  
11 a match line and wherein a most significant compare circuit of the plurality of compare  
12 circuits is coupled to the match line, the most significant compare circuit including  
13 circuitry to affect a logical state of the match line if either (1) a most significant bit of  
14 the first comparand value is less than the most significant bit of the lower value, or  
15 (2) the most significant bit of the first comparand is equal to the most significant bit  
16 of the lower value, and a result signal from a less significant compare circuit of the  
17 plurality of compare circuits indicates that the first comparand value minus the value  
18 represented by the most significant bit of the first comparand value is less than the  
19 lower value minus the value represented by the most significant bit of the lower  
20 value.

- 1 15. (currently amended) A content addressable memory (CAM) cell comprising:  
2 a first storage circuit to store a first boundary value;  
3 a first compare circuit to compare a comparand value to a the first boundary value, the first  
4 compare circuit including circuitry to output a first result signal in a first state if the  
5 comparand value is greater than the first boundary value and in a second state if the  
6 comparand value is less than the first boundary value; and

7 an input to receive a second result signal from another CAM cell, and wherein the circuitry  
8 to output the first result signal in the first state is adapted to output the first result  
9 signal in the first state if the comparand value is equal to the first boundary value and  
10 the second result signal is in the first state.

1 16. (canceled)

1 17. (previously presented) The CAM cell of claim 15 wherein the circuitry to output the first  
2 result signal is further adapted to output the first result signal in the second state if the  
3 comparand value is equal to the first boundary value and the second result signal is in the  
4 second state.

1 18. (original) The CAM cell of claim 15 further comprising:  
2 a second storage circuit to store a second boundary value; and  
3 a second compare circuit to compare the comparand value to the second boundary value,  
4 the second compare circuit including circuitry to output a second result signal in the  
5 first state if the comparand is less than the second boundary value and in the second  
6 state if the comparand is greater than the second boundary value.

1 19. (original) The CAM cell of claim 18 further comprising an input to receive a third result  
2 signal from a less significant CAM cell, and wherein the circuitry to output the second  
3 result signal in the first state is further adapted to output the second result signal in the first  
4 state if the comparand value is equal to the second boundary value and the third result  
5 signal is in the first state.

1 20. (original) The CAM cell of claim 15 wherein the circuitry to output the first result signal is  
2 adapted to output the first result signal in the first state if the comparand is equal to the first  
3 boundary value.

1 21. (original) The CAM cell of claim 15 wherein the circuitry to output the first result signal is  
2 adapted to output the first result signal in the second state if the comparand is equal to the  
3 first boundary value.

1 22. (original) The CAM cell of claim 15 wherein the first boundary value is an upper  
2 boundary value.

1 23. (currently amended) A content addressable memory (CAM) device comprising:  
2 a first storage circuit to store a first value; and  
3 a compare circuit coupled to the first storage circuit to receive the first value and coupled to  
4 a mode signal line to receive a mode signal, the compare circuit being adapted to  
5 compare a comparand value to the first value and to output a first result signal, the  
6 first result signal indicating whether the comparand value is greater than the first  
7 value when the mode signal is in a first state, and the first result signal indicating  
8 whether or not the comparand is equal to the first value when the mode signal is in a  
9 second state.

1 24. (original) The CAM device of claim 23 further comprising a second storage circuit to store  
2 a second value and coupled to provide the second value to the compare circuit, the compare

3 circuit including circuitry to compare the comparand value to the second value and to  
4 output a second result signal, the second result signal indicating whether the comparand is  
5 less than the second value when the mode signal is in the first state.

1 25. (original) The CAM device of claim 23 further comprising:

2 a second storage circuit to store a second value and coupled to provide the second value to  
3 the compare circuit, the compare circuit including circuitry to compare the  
4 comparand value to the second value and, when the mode signal is in the first state, to  
5 output a second result signal indicating whether the comparand is less than the second  
6 value; and  
7 a mask circuit coupled to receive the second value from the storage circuit and coupled to  
8 the compare circuit, the mask circuit being adapted to selectively mask the first result  
9 signal, according to the second value, when the mode signal is in the second state.

1 26. (original) The CAM device of claim 25 wherein the mask circuit is adapted to mask the  
2 first result signal by preventing the compare circuit from outputting the first result signal in  
3 a state indicative of inequality between the first value and the comparand.

1 27. (original) The CAM device of claim 25 wherein the mask circuit is adapted to mask the  
2 first result signal by disabling the first value from being received in the compare circuit.

1 28. (original) The CAM device of claim 25 wherein the mask circuit is adapted to mask the  
2 first result signal by disabling the comparand value from being received in the compare  
3 circuit.

1 29. (original) A content addressable memory (CAM) device comprising:

2 a first storage circuit to store a first value; and

3 a first compare circuit coupled to receive the first value from the first storage circuit and

4 having a select input to receive a level select signal, the first compare circuit being

5 adapted to compare a comparand value to the first value and to assert a beyond-

6 boundary signal if the level select signal is in a first state and if the comparand value

7 is greater than the first value, the first compare circuit being further adapted to assert

8 the beyond-boundary signal if the level select signal is in a second state and if the

9 comparand value is less than the first value.

1 30. (previously presented) The CAM device of claim 29 further comprising:

2 a first input to receive a first signal representative of the comparand value;

3 a second input to receive a second signal representative of a complement of the comparand

4 value; and

5 a select circuit coupled to the first input and the second input to select, according to a state

6 of the level select signal, either the first signal or the second signal to be output to the

7 compare circuit for comparison with the first value.

1 31. (original) The CAM device of claim 30 wherein the select circuit is a multiplexer having a

2 control input coupled to receive the level select signal and having first and second ports

3 coupled respectively to the first and second inputs.

1 32. (original) The CAM device of claim 29 wherein the first value is representative of an



2 upper boundary value when the level select signal is in the first state, and wherein the first  
3 value is representative of a lower boundary value when the level select signal is in the  
4 second state

1 33. (original) The CAM device of claim 29 further comprising a mode select input to receive a  
2 mode select signal, the first compare circuit being enabled to assert the beyond-boundary  
3 signal if the mode select signal is in a first state and the first compare circuit being disabled  
4 from asserting the beyond-boundary signal if the mode select signal is in a second state.

1 34. (original) The CAM device of claim 33 further comprising a second compare circuit to  
2 compare the comparand value and the first value and to assert a match signal indicative of  
3 whether the comparand value is equal to the first value, the second compare circuit being  
4 enabled to assert the match signal if the mode select signal is in the second state, and the  
5 second compare circuit being disabled from asserting the match signal if the mode select  
6 signal is in the first state.

1 35. (currently amended) A content addressable memory (CAM) device comprising:  
2 a CAM array having a plurality of CAM cells; and  
3 at least one mode select line coupled to at least one set of CAM cells within the plurality of  
4 CAM cells, the set of CAM cells being adapted to compare a comparand value to a  
5 range defined, at least in part, by at least one boundary a first value stored within the  
6 set of CAM cells if a mode select signal on the mode select line is in a first state, and  
7 the set of CAM cells being adapted to ~~compare the~~ determine whether or not the

8 comparand value ~~for equality with~~ this equal to a data value stored within the set of  
9 ~~CAM cells~~ the first value if the mode select signal is in a second state.

1 36. (original) The CAM device of claim 35 further comprising a mode configuration circuit  
2 coupled to the mode select line, the mode configuration circuit including a storage circuit  
3 to store a mode value, the mode select signal being in either the first state or the second  
4 state according to the mode value.

1 37. (original) The CAM device of claim 36 further comprising an interface to receive a first  
2 instruction from a host processor, the CAM device being adapted to store the mode value in  
3 the storage circuit in response to the first instruction.

1 38. (original) The CAM device of claim 36 further comprising a mode select interface, and  
2 wherein the mode select line is coupled to the mode select interface to receive the mode  
3 select signal from an external device.

1 39. (original) The CAM device of claim 38 wherein the external device is a host processor.

1 40. (currently amended) A system comprising:

2 a processor; and

3 a content addressable memory (CAM) device coupled to receive instructions and data

4 values from the processor, the CAM device including a plurality of CAM cells and

5 being responsive to a first instruction from the processor to select either a first

6 operating mode or a second operating mode for the plurality of CAM cells, the

7 plurality of CAM cells being adapted to compare a comparand value to a range  
8 defined, at least in part, by at least one boundary a first value stored within the  
9 plurality of CAM cells if the first operating mode is selected, and the plurality of  
10 CAM cells being adapted to ~~compare~~ determine whether or not the comparand value  
11 ~~for equality with a value equal to the first data value stored within the plurality of CAM~~  
12 ~~cells if the second operating mode is selected.~~

1 41. (original) The system of claim 40 wherein the CAM device includes a mode configuration  
2 circuit to store a mode select value in response to the first instruction, the mode select value  
3 indicating the first operating mode or the second operating mode according to the first  
4 instruction.

1 42. (original) The system of claim 41 wherein the plurality of CAM cells is responsive to the  
2 mode select value to operate in either the first operating mode or the second operating  
3 mode.

1 43. (previously presented) The system of claim 41 wherein the CAM device includes  
2 additional CAM cells configured to operate only in the first operating mode.

1 44. (original) The system of claim 41 wherein the CAM device includes additional CAM cells  
2 configured to operate only in the second operating mode.

1 45. (currently amended) A system comprising:  
2 a processor; and

3 a content addressable memory (CAM) device coupled to receive instructions from the  
4 processor, the CAM device including a first plurality of CAM cells and being  
5 responsive to a first instruction from the processor to store a first boundary value in  
6 the first plurality of CAM cells, the first plurality of CAM cells being adapted to  
7 compare the first boundary value with a first comparand value in a compare operation  
8 and to output a first result signal indicative of whether the first comparand value is  
9 greater than the first boundary value, wherein the first plurality of CAM cells are  
10 responsive to a mode select signal to operate in either a range mode or a ternary  
11 mode, the first plurality of CAM cells being adapted to output the first result signal  
12 when operated in the range mode.

1 46. (canceled)

1 47. (currently amended) ~~The system of claim 45~~ A system comprising:

2 a processor; and

3 a content addressable memory (CAM) device coupled to receive instructions from the

4 processor, the CAM device including a first plurality of CAM cells and being

5 responsive to a first instruction from the processor to store a first boundary value in

6 the first plurality of CAM cells, the first plurality of CAM cells being adapted to

7 compare the first boundary value with a first comparand value in a compare operation

8 and to output a first result signal indicative of whether the first comparand value is

9 greater than the first boundary value, wherein the first plurality of CAM cells are

10 responsive to a mode select signal to operate in either a range mode or a binary mode,

the first plurality of CAM cells being adapted to output the first result signal when operated in the range mode.

48. (currently amended) ~~The system of claim 45 wherein the CAM device further includes A~~  
system comprising:

a processor; and

a content addressable memory (CAM) device coupled to receive instructions from the  
processor, the CAM device including:

a first plurality of CAM cells and being responsive to a first instruction from the  
processor to store a first boundary value in the first plurality of CAM cells, the  
first plurality of CAM cells being adapted to compare the first boundary value  
with a first comparand value in a compare operation and to output a first result  
signal indicative of whether the first comparand value is greater than the first  
boundary value; and

a second plurality of CAM cells to store a data value, the second plurality of CAM  
cells being adapted to compare the data value with a second comparand value in  
a compare operation and to output a first result signal indicative of whether the  
second comparand value is equal to the data value.

49. (original) The system of claim 48 wherein the first plurality of CAM cells and the second  
plurality of CAM cells are each included within a first row of CAM cells within the CAM  
device.

1 50. (original) The system of claim 48 wherein the first comparand value and the second  
2 comparand value each constitute a respective field of bits within a third comparand value.

1 51. (original) The system of claim 45 wherein the CAM device is further responsive to the  
2 first instruction from the processor to store a second boundary value in the first plurality of  
3 CAM cells, and the first plurality of CAM cells being further adapted to compare the  
4 second boundary value with the second comparand in the compare operation and to output  
5 a second result signal indicative of whether the first comparand value is less than the  
6 second boundary value.

1 52. (currently amended) ~~The system of claim 45~~ A system comprising:  
2 a processor; and  
3 a content addressable memory (CAM) device coupled to receive instructions from the  
4 processor, the CAM device including a first plurality of CAM cells and being  
5 responsive to a first instruction from the processor to store a first boundary value in  
6 the first plurality of CAM cells, the first plurality of CAM cells being adapted to  
7 compare the first boundary value with a first comparand value in a compare operation  
8 and to output a first result signal indicative of whether the first comparand value is  
9 greater than the first boundary value, wherein the CAM device includes multiple  
10 independently searchable storage blocks each including a plurality having multiple  
11 rows of CAM cells therein, the first plurality of CAM cells being included within the  
12 plurality one of the rows of CAM cells in one of the searchable storage blocks.

1 53. (original) The system of claim 52 wherein the CAM device further includes a block  
2 configuration circuit to store a block configuration value, and circuitry to configure at least  
3 one of the storage blocks to have a storage width and depth according to the block  
4 configuration value.

1 54. (original) The system of claim 53 wherein the CAM device is responsive to a second  
2 instruction from the processor to store the block configuration value in the block  
3 configuration circuit.

1 55. (original) The system of claim 53 wherein the block configuration circuit is adapted to  
2 store a mode value, and wherein the first plurality of CAM cells are responsive to the mode  
3 value to operate in either a range mode or a ternary mode, the first plurality of CAM cells  
4 being adapted to output the first result signal when operated in the range mode.

1 56. (original) The system of claim 55 wherein the CAM device is responsive to a second  
2 instruction from the processor to store the mode value in the block configuration circuit.

1 57. (original) The system of claim 53 wherein the block configuration circuit is adapted to  
2 store a mode value, and wherein the first plurality of CAM cells are responsive to the mode  
3 value to operate in either a range mode or a binary mode, the first plurality of CAM cells  
4 being adapted to output the first result signal when operated in the range mode.

1 58. (currently amended) A method of operation within a content addressable memory (CAM)

2 device, the method comprising:

3 comparing a comparand value with a first ~~boundary~~-value stored in a plurality of CAM

4 cells within the CAM device; and

5 asserting a first result signal if (1) the comparand value is ~~greater than the~~within a range

6 defined, at least in part, by the first ~~boundary~~-value, and (2) a mode signal is in a first

7 state; and

8 asserting the first result signal if (1) the comparand value matches the first value, and (2)

9 the mode signal is in a second state.

1 59. (currently amended) The method of claim 58 further comprising storing the first ~~boundary~~  
2 value in the plurality of CAM cells in response to a write instruction.

1 60. (currently amended) The method of claim 58 wherein, when the mode signal is in the first  
2 state, comparing the comparand value with the first ~~boundary~~-value comprises, in each  
3 CAM cell of the plurality of CAM cells, asserting a greater-than signal if either (1) a bit of  
4 the comparand value received within the CAM cell is greater than a bit of the first  
5 boundary value stored within the CAM cell, or (2) the bit of the comparand value is equal  
6 to the bit of the first boundary value and a greater-than signal is received from a less  
7 significant CAM cell within the plurality of CAM cells.

1 61. (currently amended) The method of claim 58 wherein, when the mode signal is in the first  
2 state, a greater-than signal asserted by a most significant one of the plurality of CAM cells  
3 constitutes the first result signal.



1 62. (currently amended) The method of claim 58 further comprising:

2 comparing a comparand value with a second ~~boundary~~-value stored in the plurality of CAM  
3 cells; and  
4 asserting a second result signal if the comparand value is less than the second ~~boundary~~  
5 value.

1 63. (currently amended) The method of claim 62 wherein comparing the comparand value

2 with the second ~~boundary~~-value comprises, in each CAM cell of the plurality of CAM  
3 cells, asserting a less-than signal if either (1) a bit of the comparand value received within  
4 the CAM cell is less than a bit of the second ~~boundary~~-value stored within the CAM cell, or  
5 (2) the bit of the comparand value is equal to the bit of the second ~~boundary~~-value and a  
6 less-than signal is received from a less significant CAM cell within the plurality of CAM  
7 cells.

1 64. (original) The method of claim 63 wherein a less-than signal asserted by a most significant  
2 one of the plurality of CAM cells constitutes the second result signal.

1 65. (currently amended) A content addressable memory (CAM) device comprising:

2 means for comparing a comparand value with a first ~~boundary~~-value stored in a plurality of  
3 CAM cells within the CAM device; and  
4 means for asserting a first result signal if (1) the comparand value is greater than the first  
5 boundary value within a range defined, at least in part, by the first value and (2) a  
6 mode signal is in a first state; and

7 | means for asserting the first result signal if (1) the comparand matches the first value, and  
8 | (2) the mode signal is in a second state.

1 | 66. (currently amended) The CAM device of claim 65 further comprising means for storing  
2 | the first ~~boundary~~ value in the plurality of CAM cells in response to a write instruction.

1 | 67. (currently amended) The CAM device of claim 65 wherein the means for comparing a  
2 | comparand value with a first ~~boundary~~ value comprises respective means within each CAM  
3 | cell of the plurality of CAM cells for asserting a greater-than signal if either (1) a bit of the  
4 | comparand value received within the CAM cell is greater than a bit of the first ~~boundary~~  
5 | value stored within the CAM cell, or (2) the bit of the comparand value is equal to the bit  
6 | of the first ~~boundary~~ value and a greater-than signal is received from a less significant  
7 | CAM cell within the plurality of CAM cells.

1 | 68. (currently amended) The CAM device of claim 65 further comprising:  
2 | means for comparing a comparand value with a second ~~boundary~~ value stored in the  
3 | plurality of CAM cells; and  
4 | means for asserting a second result signal if the comparand value is less than the second  
5 | ~~boundary~~ value.

1 | 69. (currently amended) The CAM device of claim 68 wherein the means for comparing a  
2 | comparand value with a second ~~boundary~~ value comprises respective means within each  
3 | CAM cell of the plurality of CAM cells for asserting a less-than signal if either (1) a bit of  
4 | the comparand value received within the CAM cell is less than a bit of the second ~~boundary~~

value stored within the CAM cell, or (2) the bit of the comparand value is equal to the bit of the second boundary value and a less-than signal is received from a less significant CAM cell within the plurality of CAM cells.

70. (currently amended) A CAM device comprising:

at least one range compare cell configured to store a bit of a range limit, wherein the at least one range compare cell is further configured to output a first result signal that indicates ~~at least whether~~ a first bit of a comparand is outside of a range defined by the bit of the range limit ~~the stored range limit bit is greater than or less than a corresponding bit of a comparand;~~ and

at least one CAM cell configured to store a data bit, wherein the at least one CAM cell is further configured to output a match signal that indicates whether the stored data bit matches a ~~corresponding~~ second bit of a ~~the~~ comparand, wherein at least one range compare cell and at least one CAM cell are coupled to a common match line.

71. (previously presented) The CAM device of claim 70 wherein the at least one CAM cell comprises a ternary CAM cell.

72. (previously presented) The CAM device of claim 70 wherein the at least one CAM cell comprises a binary CAM cell.

73. (previously presented) The CAM device of claim 70 wherein the at least one range compare cell comprises a configurable cell that selectively operates in one of a range compare cell mode and a ternary CAM cell mode.

1 74. (previously presented) The CAM device of claim 70 wherein the at least one range  
2 compare cell comprises a configurable cell that selectively operates in one of a range  
3 compare cell mode and a binary CAM cell mode.

1 75. (previously presented) The CAM device of claim 70 wherein the at least one range  
2 compare cell comprises:  
3 at least one less significant range compare cell configured to output the result signal to a  
4 next more significant range compare cell, wherein the result signal is dependent on a  
5 result of a comparison of the stored range limit bit and the corresponding comparand  
6 bit, and a result signal output from a next less significant range compare cell; and  
7 a most significant range compare cell configured to output a final result signal to the  
8 common match line, wherein the final result signal indicates at least whether the  
9 comparand is greater than or less than the stored range limit.

1 76. (previously presented) The CAM device of claim 70 wherein the result signal further  
2 indicates whether the stored range limit bit is equal to a corresponding comparand bit .

1 77. (previously presented) The CAM device of claim 75 wherein the final result signal output  
2 to the common match line further indicates whether the stored range limit is equal to the  
3 comparand.

1 78. (currently amended) A method for performing a range comparison operation in a content  
2 addressable memory (CAM) device to determine whether a comparand is within a range,

3 the method comprising:

4 storing a first value at least one range limit in a plurality of range compare cells, including

5 a most significant range compare cell, and a plurality of less significant range

6 compare cells for storing bits of the range limit first value according to their

7 significance;

8 comparing bits of the comparand with corresponding bits of the range limit first value;

9 outputting a result signal for each range compare cell based on the bit comparison, and on a

10 result signal output by a next less significant range compare cell; and

11 outputting a final result signal from the most significant range compare cell to a match line,

12 wherein the final result signal indicates at least whether the comparand is greater than

13 or less than the range limit first value, wherein the plurality of range compare cells

14 comprises a plurality of configurable cells, including a most significant configurable

15 cell, and a plurality of less significant configurable cells for storing bits of the first

16 value according to their significance, the method further comprising, setting a mode

17 select signal to select a range compare mode or a ternary CAM mode, wherein, in the

18 ternary CAM mode, the first value comprises a data word and a mask word, and

19 wherein, in the range compare mode, the first value comprises at least one of an

20 upper range limit and a lower range limit.

1 79. (currently amended) The method of claim 78 wherein the ~~at least one range limit~~ includes  
2 ~~an upper range limit, and wherein the final result signal indicates the comparand is within~~  
3 ~~the range when, in the range compare mode, the comparand is less than the upper range~~  
4 ~~limit.~~

1 80. (currently amended) The method of claim 78 wherein ~~the at least one range limit includes~~  
2 ~~a lower range limit, and wherein the final result signal indicates the comparand is within~~  
3 the range when, in the range compare mode, the comparand is greater than the lower range  
4 limit.

1 81. (currently amended) The method of claim 78 wherein ~~the at least one range limit includes~~  
2 ~~an upper range limit, and wherein the final result signal indicates the comparand is within~~  
3 the range when, in the range compare mode, the comparand is less than the upper range  
4 limit or equal to the upper range limit.

1 82. (currently amended) The method of claim 78 wherein ~~the at least one range limit includes~~  
2 ~~a lower range limit, and wherein the final result signal indicates the comparand is within~~  
3 the range when, in the range compare mode, the comparand is greater than or equal to the  
4 lower range limit.

1 83. (currently amended) The method of claim 78 wherein ~~the at least one range limit includes~~  
2 ~~a lower range limit and an upper range limit, and wherein the final result signal indicates~~  
3 the comparand is within the range when, in the range compare mode, the comparand is  
4 greater than the lower range limit and less than the upper range limit.

1 84. (currently amended) The method of claim 78 wherein ~~the at least one range limit includes~~  
2 ~~a lower range limit and an upper range limit, and wherein the final result signal indicates~~  
3 the comparand is within the range when, in the range compare mode, the comparand is

greater than or equal to the lower range limit and less than or equal to the upper range limit.

85. (canceled)

86. (currently amended) The method of claim ~~85~~78, further comprising:

in the ternary CAM mode,

comparing a comparand bit with a masked data bit in each of the plurality of  
configurable cells; and

outputting a result signal based on the comparison from each configurable cell to the  
common match line; and

in the range compare mode,

comparing a comparand bit with an upper range bit in each of the plurality of  
configurable cells;

comparing a comparand bit with a lower range bit in each of the plurality of  
configurable cells;

outputting a first result signal from each less significant configurable cell to a next  
more significant configurable cell based on the lower range comparison and on a  
first result signal from a next less significant configurable cell;

outputting a second result signal from each less significant configurable cell to a next  
more significant configurable cell based on the upper range comparison and on a  
second result signal from the next less significant configurable cell;

outputting a first final result signal from the most significant configurable cell to the  
common match line based on based on the lower range comparison and on a first

20 result signal from a next less significant configurable cell; and  
21 outputting a second final result signal from the most significant configurable cell to  
22 the common match line based on the upper range comparison and on a second  
23 result signal from the next less significant configurable cell.

1 87. (canceled)